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10/623,732	07/22/2003	Kyoichi Suguro	04329.2344-02	6071

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER

LOKE, STEVEN HO YIN

ART UNIT PAPER NUMBER

2811

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/623,732

Applicant(s)

SUGURO ET AL.

Examiner

Steven Loke

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 34-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 34-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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1. Claims 3-5, 34, 37, 38 and 39 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 12 discloses the element isolating insulating film [62] having a top surface projecting upward above a top surface of the semiconductor layer [61]. It further discloses the top surface position of said element isolating insulating film [62] is not higher than a top surface position of the gate electrode [64]. However, the specification never discloses the gate electrode is a metal gate electrode, and said gate insulating film being formed on a top surface and sides of the semiconductor layer in each of said element regions which are not covered with said element isolating insulating film as claimed in claims 38 and 39.

The specification never discloses a metal gate electrode as claimed in claim 3.

Fig. 12 and the specification (page 54, lines 14-19) disclose the top surface of the element isolating insulating film is higher than top surface of the gate insulating film and the step amount is at least three times as large as the thickness of the gate oxide film. However, the specification never discloses the difference in height from said substrate between a top surface position of said semiconductor layer and a top surface position of said element isolating insulating film is at least three times as large as a thickness of said gate

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insulating film when the element isolating insulating film having a top surface which is lower than a top surface of semiconductor layer as claimed in claim 4.

The specification never discloses the difference in height from said substrate between the top surface position of said semiconductor layer and a top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region when the element isolating insulating film having a top surface which is lower than a top surface of semiconductor layer as claimed in claim 5.

The specification never discloses said element isolating insulating film and said gate insulating film are formed in different steps as claimed in claim 34.

The specification never discloses said element isolating insulating film is a thermally grown oxide film as claimed in claim 37.

2. Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4, lines 2-3, claim 5, line 3, the phrase "a top surface position of said semiconductor layer" is unclear whether it is being referred to a top surface of said semiconductor layer in line 7 of claim 3.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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4. Claims 1, 2, 35 and 36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamazaki.

In regards to claim 1, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103] and a trench (the area occupied by the oxide film [113, 115c, 116a] (fig. 8c)), said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [113, 115c, 116a] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; wherein the element isolating insulating film [113, 115c, 116a] is an oxide film; and a MOS type element formed within a corresponding one of the element regions and having a gate insulating film [118] and a gate electrode [122a] on the gate insulating film [118], wherein: a difference in height from the substrate between a top surface position of said element isolating insulating film and a top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film, the top surface position of said element isolating insulating film is not higher than a top surface position of the gate electrode [122a], and said element isolating insulating film [113, 115c, 116a] and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

In regards to claim 2, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103] and a trench (the area occupied by the oxide film [113, 115c, 116a] (fig. 8c)), said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [113, 115c, 116a] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a top surface of the semiconductor layer; wherein the element isolating insulating film [113, 115c, 116a] is an oxide film; and a MOS type element formed within a corresponding one of said element regions and having a gate insulating film [118], wherein: a difference in height from the substrate between a top surface position of the element isolating insulating film and a top surface position of the semiconductor layer is at least 10 nm because the height of the top portion of the insulating film [113, 115c, 116a] is larger than the thickness of the gate insulating film [118] (col. 15, lines 10-14). It further discloses the top surface position of said element isolating insulating film [113, 115c, 116a] is not higher than a top surface position of a gate electrode [122a], and said element isolating insulating film [113, 115c, 116a] and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

In regards to claims 35 and 36, Yamazaki further discloses a portion of said element isolating insulating film [113] is a thermally grown oxide film (col. 11, lines 9-11).

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5. Claims 3, 4, 34 and 37 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Miyawaki et al.

In regards to claim 3, Miyawaki et al. show all the elements of the claimed invention in figs. 33, 10 and 14. It is a semiconductor device, comprising: a substrate [1012, 1013, 1016, 1021] having a semiconductor layer [1013, 1016, 1021] and a trench (the area occupied by layer [1091']), said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [1091'] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface which is lower than a top surface of said semiconductor layer; and a MOS type element (figs. 33 and 14) formed within a corresponding one of said element regions and having a gate insulating film (the layer with the dots) and a metal gate electrode ([1069] is made of tungsten silicide (col. 10, lines 10-15)) formed thereon, wherein: said gate insulating film is formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film [1091'], said gate electrode is formed on said gate insulating film, and, a top surface position of said element isolating insulating film [1091'] is not higher than a top surface position of the gate electrode [1069], and said element isolating insulating film (the vertical portion of layer [1091']) and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

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The process limitation of how the semiconductor layer is formed has no patentable weight in claim drawn to structure. Note that a product by process claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a product by process claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Therefore, the phrase "epitaxial layer" is thus non-limiting.

In regards to claim 4, Miyawaki et al. further disclose the difference in height from said substrate between the top surface position of said semiconductor layer and a top surface position of said element isolating insulating film [1091'] is at least three times as large as a thickness of said gate insulating film.

In regards to claim 34, Miyawaki et al. disclose said element isolating insulating film [1091'] and said gate insulating film (the layer with the dots).

The process limitation of how said element isolating insulating film and said gate insulating film are formed have no patentable weight in claim drawn to structure. Note that a product by process claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See

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also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a product by process claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Therefore, the phrase "formed in different steps" is thus non-limiting.

In regards to claim 37, Miyawaki et al. disclose said element isolating insulating film [1091'] is an oxide film.

The process limitation of how said element isolating insulating film is formed has no patentable weight in claim drawn to structure. Note that a product by process claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a product by process claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether

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claimed in product by process claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Therefore, the phrase "thermally grown" is thus non-limiting.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki et al.

In regards to claim 5, Miyawaki et al. further disclose the MOS element inherently includes a source/drain region because MOS transistor must has a source/drain region.

Miyawaki et al. differ from the claimed invention by not showing the difference in height from said substrate between a top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region.

It would have been obvious for the difference in height from said substrate between a top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region because it depends on the resistance of the source/drain region.

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8. Applicant's arguments filed 1/30/06 have been fully considered but they are not persuasive.

It is urged, in page 10 of the remarks, that the specification (page 42, lines 4-5) describes a metal gate electrode. However, the metal gate is only for the embodiment in fig. 4K. The specification never discloses the metal gate is good for the embodiment in figs. 17A-19C.

It is urged, in page 10 of the remarks, that the specification (page 54, lines 10-12) discloses the structure as shown in fig. 12 "is formed using, for example, any of the first to tenth embodiments". However, the specification (page 54, lines 10-12) discloses the silicon layer 61 is formed using, for example, any of the first to tenth embodiments. It never discloses the embodiment of figs. 17A-19C can be used in any of the first to tenth embodiments. Therefore, claims 3-5, 34 and 37-39 are still rejected under 35 USC 112, first paragraph.

It is urged, in page 12 of the remarks, that the silicon oxide films 113 and 116a of Yamazaki are not used to isolate or insulate element regions in semiconductor layer 103. It also urged that Yamazaki only teaches that BPSG film 115c can be used as an element insulating film. However, silicon oxide films 113 and 116a are insulating elements which are considered as parts of the insulate element regions in semiconductor layer 103. Therefore, silicon oxide films 113 and 116a, and BPSG film 115c are considered as an element isolating insulating film. Yamazaki does disclose the element isolating insulating film [113, 115c, 116a] having a top surface projecting upward above a top surface of said semiconductor region [103].

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It is urged, in pages 12-14 of the remarks, that the area occupied by field oxidized film 1091' of Miyawaki is not a trench. However, Miyawaki clearly discloses a trench formed between two mesas which are formed by semiconductor layers [1013, 1016, 1021]. Since there is a trench in Miyawaki device, Miyawaki teaches the element isolating insulating film [1091'] provided in the trench for partitioning the semiconductor layer [1013, 1016, 1021] into a plurality of element regions.

It is urged, in pages 13-14 of the remarks, that an interior side of field oxidized film 1091' is curved. In addition, an interface between field oxidized film 1091' and the region occupied by p+ layer 1013, p layer 1016, and p- layer (collectively, an element region) is curved. However, fig. 33 clearly discloses layer [1091'] has two vertical portions formed adjacent to layers [1013, 1016, 1021]. The sidewalls of the vertical portions are in direct contact with the layers [1013, 1016, 1021]. Therefore, Miyawaki does disclose said element isolating insulating film [1091'] and each of said element regions [1013, 1016, 1021] make an interface which is substantially perpendicular to the top surface of said semiconductor layer [1013, 1016, 1021].

It is urged, in pages 14-15 of the remarks, that Miyawaki does not disclose the element isolating insulating film provided in the trench for partitioning the semiconductor layer into a plurality of element regions. However, as mentioned in the previous paragraph, Miyawaki does disclose the element isolating insulating film [1091'] provided in the trench for partitioning the semiconductor

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layer [1013, 1016, 1021] into a plurality of element regions. Therefore, claim 5 is still obvious over Miyawaki.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
April 14, 2006

Steven Lohr